IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	January 14, 2009
Kubo, et al	Group Art Unit: 2621
Serial No. 10/716,791	Examiner: David Werner
Filed: November 19, 2003	IBM Corporation Anne Vachon Dougherty 3173 Cedar Road Yorktown Hts, NY 10598
Title: FORMAT CONVERSION CIRCUIT	

Board of Patent Appeals and Interferences
Alexandria, VA 22313-1450

Response To Notice of Non-Compliant Appeal Brief

In response to the Notice of Non-Compliant Appeal Brief dated January 7, 2009 for the referenced application under appeal, Appellants have amended the sections that were found to be defective. As per the Notice, only the amended sections need to be submitted.

Attached herewith are amended sections entitled:

III. STATUS OF CLAIMS and

V. SUMMARY OF CLAIMED SUBJECT MATTER.

Respectfully submitted,
Kubo, et al
By: /Anne Vachon Dougherty/
Anne Vachon Dougherty
Registration No. 30,374
Tel. (914) 962-5910

III. STATUS OF CLAIMS

There are seven (7) claims pending in the subject patent application, numbered 1-7. Claims 1-7 have been finally rejected. No claims stand allowed. A complete copy of the claims involved in the appeal is attached hereto.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1

Independent Claim 1 recites a formal conversion circuit (100 of Fig. 8) for conversion of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, including a memory for storing video data (FIFO 101 of Fig. 8 and page 11, lines 14-20), header generation device for generating a packet header that adheres to a standard for motion picture compression (Header generation circuit 102 of Fig. 8 and page 11, lines 21-24), synchronous timing detector for detecting a synchronizing signal for a line of video data (Circuit 103 of Fig. 8 and page 11, lines 25-29) and a selection device (counter 104 and switch 105 and page 11, line 30-page 12, line 23) for repeating the selection of the packet header generated by said header generation means and selection of a predetermined amount of video data read out of said memory (page 14, lines 1-10) as a payload responsive to the packet header, during an

interval from when said synchronous timing detection device detects the synchronizing signal for the line of data until it detects the next synchronizing signal at a start of a next successive line of data (page 13, lines 1-3), whereby for each line of data, the selection of video data is completed during the horizontal synchronizing period following that line of data (page 10, lines 12-14; Fig. 7).

Independent Claim 6

Claim 6 recites a format conversion method (Fig. 7) for converting the format of digitized video data, comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, comprising steps of storing video data (page 11, lines 14-15); generating a packet header that adheres to a standard for motion picture compression (page 11, lines 21-24); detecting a synchronization signal for a line of the video data (page 11, lines 25-29); and repeating (page 14, line 11) the generation of a packet header and selecting a predetermined amount of the video data (page

14, lines 1-10) as a payload responsive to latter said packet header (page 11, line 30-page 12, line 23 and page 13, lines 25-31), during an interval between detection of a synchronization signal for the line of data and detection of a synchronization signal for a successive line of data (page 13, lines 1-3) whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data (page 10, lines 12-14).

Independent Claim 7

Claim 7 recites a computer readable storage device encoded with a computer program to perform a format conversion method. for converting the format of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, said method comprising steps of storing video data (page 11, lines 14-15); generating a packet header that adheres to a standard for motion picture compression (page 11, lines 21-24); detecting a synchronization signal for a line of the video data (page 11, lines 25-

29); and repeating (page 14, line 11) the generation of a packet header and selecting a predetermined amount of the video data (page 14, lines 1-10) as a payload responsive to latter said packet header (page 11, line 30-page 12, line 23 and page 13, lines 25-31), during an interval between detection of a synchronization signal for the line of data and detection of a synchronization signal for a successive line of data (page 13, lines 1-3) whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data (page 10, lines 12-14).

Dependent Claim 2

As recited in Claim 2, the selection device of the format conversion circuit includes a counter (104 of Fig. 8), reset in response to the synchronizing signal detected by said synchronous timing detector, for counting the amount of packet header output from said header generation device and the amount of video data read out of said memory, and a switch (105 of Fig. 8), which selects the packet header generated by said header

generation device until the amount of packet header counted by said counter reaches a predetermined amount, and selects the video data read out of said memory after the amount of packet header counted by said counter has reached the predetermined amount.

Independent Claim 3

Independent Claim 3 recites a format conversion circuit (100 of Fig. 8) for converting the format of digitized video data comprising a plurality of lines of data with a plurality of horizontal synchronization periods, one horizontal synchronizing period following each line of data, to a pseudo MPEG2-TS format.

The format conversion circuit comprises a FIFO memory (101 of Fig. 8) for storing the video data in response to a clock for the video data; a header generation circuit (102 of Fig. 8) for generating an MPEG2-TS packet header in response to the clock for the video data; a synchronous timing detection circuit (103 of Fig. 8) for detecting a horizontal synchronizing signal for the video data said horizontal synchronizing signal indicating the end of a horizontal synchronizing

period for a preceding line of data and the start of a next successive line of data; a counter (104 of Fig. 8), reset in response to the horizontal synchronizing signal detected by said synchronous timing detection circuit, for counting the number of bytes of packet header output from said header generation circuit and the number of bytes of video data read out of said FIFO memory; and a switch (105 of Fig. 8), which selects the packet header generated by said header generation circuit until the number of bytes counted by said counter reaches the number of bytes of packet header as specified by MPEG2-TS, and selects the video data read out of said FIFO memory after the number of bytes counted by said counter has reached the number of bytes of packet header as specified by MPEG2-TS, whereby the switch alternately selects the packet header and the video data for successive packets until all video data for a line has been packetized and whereby, for each line of data, the selecting of video data is completed during the horizontal synchronizing period following that line of data.

Dependent Claim 4

The invention as set forth in Claim 4 further includes the feature that the counter outputs a data valid signal (page 10, lines 25-28 and page 11, lines 12-13) that indicates the validity of the data, the format of which has been converted to the pseudo MPEG2-TS format, while counting the number of bytes of packet header and the number of bytes of video data.

Dependent Claim 5

The invention as set forth in Claim 5 further includes the feature that the FIFO memory is reset in response to the data valid signal output from said counter to erase the video data stored (page 11, lines 18-20).